REMARKS

Claims 2-6 and 24-30 are pending in the present application. Replacement claims 2-6 and 24-29 have been presented herewith. Also, claim 30 has been presented herewith. Claim 23 has been canceled.

Finality of Office Action

The current Office Action dated April 29, 2002, has been made final. The Examiner has asserted on page 5 of the Final Office Action that Applicant's Amendment necessitated the new grounds of rejection presented in the Office Action.

As will be addressed in further detail subsequent to this issue of finality, the claims have been newly rejected under 35 U.S.C. 112, first paragraph. Particularly, the Examiner has asserted that the "first annealing" and the "second annealing" of the claims are not described in the specification in such a way as to reasonable convey that Applicant has possession of the claimed invention.

However, Applicant respectfully submits that these new grounds of rejection were not necessitated by Applicant's Amendment dated February 4, 2002. That is, claim 24 as pending in view of the Preliminary Amendment dated July 12, 2001, featured in combination performing "a first annealing" and performing "a second annealing". Since the language in question was present in claim 24 prior to the Amendment dated February 4, 2002, it is clear that the new grounds of rejection under 35 U.S.C. 112, first paragraph could not have been necessitated by the Amendment dated February 4, 2002.

Accordingly, the Examiner is respectfully requested to withdraw the finality of the current Office Action dated April 29, 2002, because the new grounds of rejection under 35 U.S.C. 112, first paragraph were not necessitated by Applicant's Amendment dated February 4, 2002. **The Examiner is further respectfully requested to enter the current claim amendments as being responsive to an Office Action dated April 29, 2002, which should properly be accorded non-final status.**

Claim Rejections-35 U.S.C. 112

Claims 2-6 and 23-29 have been rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey that the inventor had possession of the claimed invention at the time the application was filed. The Examiner has alleged that the specification only describes first and second rapid thermal annealing (RTA), not annealing other than RTA.

Although Applicant does not necessarily concede that the above noted rejection is proper, the claims have been amended to feature first and second rapid thermal annealings. Applicant therefore respectfully submits that the claims are in compliance with 35 U.S.C. 112, first paragraph, and respectfully urges the Examiner to withdraw this rejection.

Information Disclosur_ Statem_nt

As noted in the Amendment dated February 4, 2002, the Examiner has alleged that the Information Disclosure Statement filed on September 17, 1999, fails to comply with 37 C.F.R. §1.98(a)(3), because it does not include a concise explanation of the relevance of the non-English language document. Accordingly, the document has not been considered.

However, as set forth in 37 C.F.R. §1.98(a)(3), "The concise explanation may be either separate from the specification or incorporated therein" (our emphasis added). Applicant respectfully submits that the concise explanation of the non-English language document "Semiconductor World", as cited in the Information Disclosure Statement filed on September 17, 1999, is provided on page 1 of the present application. Applicant therefore respectfully submits that the Information Disclosure Statement filed on September 17, 1999 is in compliance with 37 C.F.R. §1.98(a)(3).

Accordingly, the Examiner is again respectfully requested to consider the non-English language document "Semiconductor World", in view of the concise explanation on page 1 of the present application, and to cite this corresponding document of record in the present application, in accordance with 37 C.F.R. §1.98(a)(3).

Claim Rejections-35 U.S.C. 103

Claims 2-6 and 23 have been rejected under 35 U.S.C. 103(a) as being

unpatentable over Applicant's admitted prior art, the Doan et al. reference (U.S. Patent No. 5,946,595), and the Besser et al. reference (U.S. Patent No. 6,165,903). Also, claims 24-29 have been rejected under 35 U.S.C. 103 as being unpatentable over Applicant's admitted prior art, the Doan et al. reference, and the Besser et al. reference, in further view of the Xiang et al. reference (U.S. Patent No. 6,015,752). These rejections, insofar as they may pertain to the presently pending claims, are traversed for the following reasons.

The method for fabricating a semiconductor device of claim 30 as presented herewith, features in combination "the semiconductor device including a p-channel MOS transistor having p-type source and drain regions, and including an n-channel MOS transistor having n-type source and drain regions". The method further features "said doping comprising doping a p-type impurity into the supplemental silicon layer that is provided over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is provided over the n-channel MOS transistor". Applicant respectfully submits that prior art as relied upon by the Examiner does not disclose or make obvious these features.

Applicant's prior art Figs. 1A-1C do not include a supplemental silicon layer. Additionally, the Examiner has characterized polysilicon layer 24 in Fig. 3 of the Doan et al. reference as a supplemental silicon layer. However, polysilicon layer 24 of the Doan et al. reference is not described or suggested as being doped with an impurity. More particularly, the Doan et al. reference does not describe doping polysilicon layer 24 with a p-type impurity over a p-channel MOS transistor and with an n-type impurity over an

n-channel MOS transistor. The Examiner has further characterized silicon layer 46 of the Besser et al. reference as a supplemental silicon layer. However, silicon layer 46 of the Besser et al. reference is not described as being doped with an impurity. More particularly silicon layer 46 is not described as being doped with a p-type impurity over a p-channel MOS transistor and an n-type impurity over an n-channel MOS transistor.

The Examiner has apparently alleged on page 5, lines 1-7 of the current Office Action that the Xiang et al. reference discloses doping a supplemental silicon layer with a p-type impurity over a p-channel MOS transistor and an n-channel impurity over an n-channel MOS transistor. The Examiner has relied on Fig. 1, layer 11a and column 4 lines 15-34 of the Xiang et al. reference as support for this apparent position.

However, as described in column 4, lines 17-21 of the Xiang et al. reference with respect to Fig. 1, the source/drain regions of the device comprise a shallow extension region 11A and a heavily doped (HD) region 11B doped with a p-type impurity. Layer 11A of the Xiang et al. reference is not a supplemental silicon layer. That is, layer 11A is merely part of a doped source/drain region of the substrate. Since the Xiang et al. reference does not include a supplemental silicon layer, the Xiang et al. reference clearly would provide no motivation to modify the previously relied upon prior art to impurity dope a supplemental silicon layer. Also, since the Xiang et al. reference does not disclose both a p-channel MOS transistor and an n-channel MOS transistor, the Xiang et al. reference clearly fails to provide the necessary motivation to dope a supplemental silicon layer with a p-type impurity over a p-channel MOS transistor and an n-type impurity over an n-channel MOS transistor.

Applicant therefore respectfully submits that the Xiang et al. reference as relied upon by the Examiner fails to overcome the above noted deficiencies of the previously relied upon prior art. Accordingly, Applicant respectfully submits that the method for fabricating a semiconductor device of claim 30 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 30 and 2-6, are improper for at least these reasons.

Applicant also respectfully submits that the method for fabricating a semiconductor device of claim 24 would not been obvious in view of the prior art as relied upon by the Examiner, for at least somewhat similar reasons as set forth above. The prior art as relied upon by the Examiner does not disclose or make obvious doping a p-type impurity into a supplemental silicon layer formed over a p-channel MOS transistor, and doping an n-type impurity into a supplemental silicon layer formed over an n-channel MOS transistor. Accordingly, Applicant respectfully submits that the method for fabricating a semiconductor device of claim 24 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that these rejections, insofar as they may pertain to claims 24-29, are improper for at least these reasons.

Conclusion

As noted above, Applicant respectfully submits that the finality of the current Office Action dated April 29, 2002, is improper. That is, the new grounds of rejection

under 35 U.S.C. 112, first paragraph were not necessitated by the Amendment dated February 4, 2002. Accordingly, since the finality of the Office Action dated April 29, 2002 is improper and should be withdrawn, the current amendments should be entered and considered.

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejections, and to pass the claims of the present application to issue, for at least the above reasons.

In the event that there are any outstanding matters remaining in the present application, the Examiner is invited to contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (703) 715-0870 in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment or credit any overpayment to Deposit Account No. 50-0238 for any additional fees required under 37 C.F.R. § 1.16 or under 37 C.F.R. § 1.17; particularly, extension of time fees.

Respectfully submitted,

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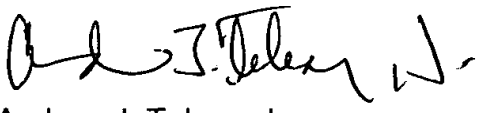

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Enclosures: Version with marked-up changes

VERSION WITH MARKED-UP CHANGES

Additions/Deletions to the Claims:

2. (Three times Amended) The method according to claim [23] 30, wherein the metal layer comprises cobalt [(Co)].

3. (Three times Amended) The method according to claim [23] 30, wherein the metal layer comprises titanium [(Ti)].

4. (Three times Amended) The method according to claim [23] 30, wherein the supplemental silicon layer is poly-silicon formed by a [CVD (Chemical Vapor Deposition)] chemical vapor deposition technique.

5. (Three times Amended) The method according to claim [23] 30, wherein the supplemental silicon layer is [a-Si (amorphous silicon)] amorphous silicon formed by a sputtering technique.

6. (Three times Amended) The method according to claim [23] 30, further comprising:

selectively removing non-reacted silicon from the second-reacted silicide region after the second rapid thermal annealing.

24. (Twice Amended) A method for fabricating a semiconductor device, comprising:

providing a semiconductor substrate which has a silicon region located on an insulating layer formed in the semiconductor substrate;

forming a metal layer on the silicon region of the semiconductor substrate;

performing a first rapid thermal annealing on the semiconductor substrate to form [a] first-reacted silicide [region] regions;

forming a supplemental silicon layer on the first-reacted silicide [region] regions;

doping an impurity into the supplemental silicon layer; and

performing a second rapid thermal annealing to convert the first-reacted silicide [region] regions into [a] second-reacted silicide [region] regions, by reaction of the supplemental silicon layer with the first-reacted silicide [region] regions,

the semiconductor device including a p-channel MOS transistor having p-type source and drain diffusion layers, and including an n-channel MOS transistor having n-type source and drain diffusion layers,

said doping comprising doping a p-type impurity into the supplemental silicon layer that is formed over the p-channel MOS transistor and doping an n-type impurity into the supplemental silicon layer that is formed over the n-channel MOS transistor.

25. (Amended) The method according to claim 24, wherein the metal layer comprises cobalt [(Co)].

26. (Amended) The method according to claim 24, wherein the metal layer comprises titanium [(Ti)].

27. (Amended) The method according to claim 24, wherein the supplemental silicon layer is poly-silicon formed by a [CVD (Chemical Vapor Deposition)] chemical vapor deposition technique.

28. (Amended) The method according to claim 24, wherein the supplemental silicon layer is [a-Si (amorphous silicon)] amorphous silicon formed by a sputtering technique.

29. (Amended) The method according to claim 24, further comprising:

selectively removing non-reacted silicon from the second-reacted silicide [region] regions after the second rapid thermal annealing.